IN THE CLAIMS

1. (Currently Amended) A method, comprising simulating from a drawn layout a photolithographic mask for fabrication of an integrated circuit, then simulating an image to be produced by that mask on a wafer.

2. (Original) The method of claim 1, further comprising correcting and/or optimizing the mask and/or the simulation of image thereof.

3. (Original) The method of claim 2 wherein said correcting and/or optimizing comprises increasing or decreasing at least one magnitude or value of (a) an optical proximity correction factor and/or (b) a serif.

4. (Currently Amended) A method, comprising simulating optical proximity effects of a drawn layout for a mask for fabrication of an integrated circuit, and correcting corner rounding effects in an image produced by said mask.

5. (Original) The method of claim 3 wherein the optical proximity effects comprise effects of light having a wavelength of approximately four times a feature size of said image.

6. (Original) A method, comprising incorporating corrections for corner rounding effects in an image produced by an integrated circuit mask into an optical proximity correcting procedure by adjusting an as-drawn layout of the mask as part of a computer aided design process.

7. (Original) The method of claim 6 wherein distortions are applied to corners and serifs in the mask.

8. (Original) A format for data input into or output from either or both simulating steps of claim 1, each format being compatible with the other.

9. (New) A method for producing a mask for fabrication of an integrated circuit, comprising:

simulating a mask from a first drawn layout, to produce a simulated mask;

comparing the simulated mask and the first drawn layout;

correcting the first drawn layout, to produce a second drawn layout; and

producing a mask from the second drawn layout;

wherein the simulating comprises simulating proximity effects and resolution due to pixel size.

10. (New) The method of claim 9, wherein the proximity effects comprise effects of light having a wavelength of approximately four times a feature size of said drawn layout.

11. (New) The method of claim 9, further comprising simulating a photoresist pattern from the simulated mask, prior to correcting the first drawn layout.

12. (New) A method of producing a semiconductor structure, comprising:

producing a mask by the method of claim 9; and

producing a semiconductor structure from the mask.

13. (New) A method of producing an integrated circuit, comprising:

producing a semiconductor structure by the method of claim 12; and

producing a integrated circuit from the semiconductor structure.